Amendments to the Claims

This listing of the claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising:

(a) a field oxide layer disposed on a semiconductor substrate and within a contact region;

(b) a metal plug contact disposed within said contact region and above said field oxide layer, wherein said metal plug contact contacts said field oxide layer, and wherein said field oxide layer electrically isolates said metal plug contact from said contact region; and

(c) a metal connected to said metal plug contact.

2. (Original) The device as claimed in claim 1, wherein said semiconducting device comprises integrated circuits.

3. (Original) The device as claimed in claim 1, wherein said field oxide layer further comprises silicon oxide.

4. (Original) The device as claimed in claim 2, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits and bipolar silicon-based integrated circuits.

5. (Currently Amended) A method for preventing and/or thwarting reverse engineering, comprising ~~steps of~~:

(a) providing a field oxide layer disposed on a semiconductor substrate and within a contact region;

(b) providing a metal plug contact disposed within said contact region and above said field oxide layer, wherein said metal plug contact contacts said field oxide layer, and wherein said field oxide layer electrically isolates said metal plug contact from said contact region; and

(c) connecting a metal to said metal plug contact.

6. (Original) The method as claimed in claim 5, wherein said semiconducting device comprises integrated circuits.

7. (Original) The method as claimed in claim 5, wherein said field oxide layer further comprises silicon oxide.

8. (Original) The method as claimed in claim 6, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits.

9. (Currently Amended) A semiconducting device adapted to prevent and/or to thwart reverse engineering, comprising:

(a) a field oxide layer disposed on a semiconductor substrate adjacent a contact region;

(b) a metal plug contact having a first surface and a second surface opposite said first surface, said metal plug contact disposed outside [[a]]said contact region, ~~and~~ wherein said second surface of said metal plug contact is disposed above said field oxide layer and in contact with a dielectric material, wherein said metal plug contact is electrically isolated from said contact region; and

(c) a metal connected to said first surface of said metal plug contact.

10. (Original) The device as claimed in claim 9, wherein said semiconducting device comprises integrated circuits.

11. (Original) The device as claimed in claim 9, wherein said field oxide layer further comprises silicon oxide.

12. (Original) The device as claimed in claim 10, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits and bipolar silicon-based integrated circuits.

13. (Currently Amended) A method for preventing and/or thwarting reverse engineering, comprising ~~steps of~~:

(a) providing a field oxide layer disposed on a semiconductor substrate adjacent a contact region;

(b) providing a metal plug contact having a first surface and a second surface opposite said first surface, said metal plug contact disposed outside [[a]]said contact region, ~~and~~ wherein said second surface of said metal plug contact is disposed above said field oxide layer and in contact with a dielectric material, wherein said metal plug contact is electrically isolated from said contact region; and

(c) connecting a metal to said first surface of said metal plug contact.

14. (Original) The method as claimed in claim 13, wherein said semiconducting device comprises integrated circuits.

15. (Original) The method as claimed in claim 13, wherein said field oxide layer further comprises silicon oxide.

16. (Original) The method as claimed in claim 14, wherein said integrated circuits further comprise complementary metal oxide-semiconductor integrated circuits.

17. (Previously Presented) The device as claimed in claim 1, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost

side of said field oxide layer.

18. (Previously Presented) The method as claimed in claim 5, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

19. (Previously Presented) The device as claimed in claim 9, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

20. (Previously Presented) The method as claimed in claim 13, wherein said field oxide layer has an uppermost side, said metal plug contact being disposed on said uppermost side of said field oxide layer.

Claims 21-22 (Canceled)

23. (currently amended) The device of claim 9, wherein ~~said metal plug contact contacts~~ said field oxide layer comprises said dielectric material.

24. (currently amended) The method of claim 13, wherein s~~aid metal plug contact contacts~~ said field oxide layer comprises said dielectric material.